Analysis and control strategy for a current-source based D-STATCOM towards minimum losses


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**ABSTRACT**

This work deals with a Distribution Static Synchronous Compensator (D-STATCOM) based on a current-source converter for low and medium voltage distribution systems, specifically small and medium manufacturers industries which are fined if the displacement power factor is below given limits. The D-STATCOM is analyzed using its mathematical model, showing the strong relation of the D-STATCOM power losses and its DC current level. Using the operating region of the D-STATCOM, an operating sub-region is defined such that the minimum DC current is used for a required reactive compensation, which leads to reducing the operating losses in the D-STATCOM. Also, Selective Elimination Harmonic is used to modulate the equipment to reduce the switching frequency while ensuring a desired current quality in the D-STATCOM input. As a result, a simple control strategy is proposed that uses a fixed modulation index while a phase control regulates the DC current to the lowest value required for reactive power compensation. Mathematical analysis jointly with simulated and experimental results corroborates the proposal, showing that it is possible to achieve a suitable compensation capability for improving the efficacy of the STATCOM.

**1. Introduction**

The main advantages of a Current Source Converter based Distribution Static Synchronous Compensator (CSC D-STATCOM) –see Fig. 1- are: (i) the simple control scheme used to control the D-STATCOM current by means of an open loop, (ii) the high efficiency for variable loads, due to the adjustable DC current capability, and (iii) the high quality in the AC STATCOM current because of the use of an LC filter; however, its main drawbacks are the power losses in the bulky DC inductor and the power valves [1–6].

Because of the power losses are a function of the DC current, \(I_{dc}\), the operation of the CSC D-STATCOM should be maintained to low values of the DC current. This is achieved using a linear area in its operating region as elaborated hereafter. This approach limits the operation region of the equipment because the DC current level defines the AC D-STATCOM state variables values and, therefore, the reactive power that the equipment can compensate. Two options to improve the efficiency of the CSC D-STATCOM are: (i) to use the LC filter design to increase the compensation capabilities and (ii) to increase the number of CSC modules connected to a common LC filter [7,8]. The first case adds a desired reactive power value for the LC filter design to displace the operating region in the reactive power axis, while the use of several CSC connected in parallel allows increasing the reactive power which can be compensated by the CSC D-STATCOM. Drawbacks are related to the cost and size of the capacitors for the first case, while the multilevel option also increases the cost, and the control scheme became more complex.

The semiconductor’s losses in a current-source topology are due to the power transfer between the AC and DC side and the zero states where one converter’s leg should be in conduction mode. Thus, the losses depend on (i) conduction voltage of the power valve, (ii) DC current level, and (iii) switching frequency [9,10]. Overcoming the DC current level losses by reducing it to the minimum value possible, the next step is to reduce the power valve losses. Indeed, they can be reduced selecting a power valve with reduced conduction voltage and an appropriate modulation technique. Selective Harmonic Elimination (SHE) is a modulation technique where the gating angles have been calculated by an off-line optimization algorithm, which ensures a reduced switching frequency, the unitary gain for the fundamental components, and a given number of harmonics eliminated in the PWM spectra [11–13]. SHE patterns are very effective suppressing unwanted harmonics of modulated current/voltages in steady-state operation. Notwithstanding the above, these characteristic impair if either: the modulating index, or the displacement angle, or the DC amplitude are

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changing within one cycle. This is not really a drawback if the control is not imposing large and repetitive changes in references [14]. On the other hand, if the process variable is noisy, the risk of getting the controller responding to the noise exists, generating AC patterns with the unwanted harmonics. To avoid that situation, different strategies must be chosen depending on the application. Simple and robust PI controllers act as low pass filter reducing noise effects for applications where fast responses are not a critical issue [15,16]. If the application needs a faster dynamic, modified algorithms were proposed in [17–20].

This work studies a CSC D-STATCOM for low and medium voltage applications, specifically for reactive power compensation in manufacturing industries which feature a high penetration of inductive loads and nonlinear loads and are limited to a minimum overall displacement power factor. These kinds of industries require dynamic and low-cost power compensation that can be achieved by a CSC based topology. To reduce the operation cost of the equipment by reducing its losses, the control strategy is focused on the DC current level minimization for the required reactive power compensation. Hence, a selective harmonic elimination technique is used jointly with a simple control scheme, ensuring a low switching frequency and low-level DC current at the same time. Importantly, the implementation of the resulting scheme does not require a high-cost digital system mainly because of the simplicity of the proposed control algorithms.

The document is arranged as follow. In Chapter II, the CSC D-STATCOM is analyzed, including its mathematical model and its operating region to define a sub-region where the proposed D-STATCOM is most efficient. Chapter III deals with the Selective Harmonic Elimination applied to the proposed D-STATCOM, focusing on its use to operate the D-STATCOM in the sub-region. Chapter IV is focused on the control scheme, including its analysis and digital implementation. Chapter V shows the analysis and simulated results for power compensation of a new laboratory building feed by 380 V/50 Hz and 150kVA installed power. Finally, Chapter IV shows the experimental results for a 3 kVA laboratory prototype to corroborate the previous analyses. Analysis and results show the feasibility of the use of a CSC D-STATCOM in an efficient way, reducing its losses and keeping an acceptable dynamic response while it losses in steady state are low.

2. Operation of a D-STATCOM based on current source converter

2.1. Mathematical model

The objective of the D-STATCOM is to inject a controlled current $i_{abc}^{\text{PCC}}$ to compensate for the unwanted components of the load current, $i_{abc}^L$, achieving a high-quality current in the point of common coupling (PCC), $i_{abc}^{\text{PCC}}$. Thus, according to Fig. 1:

\[
i_{abc}^{\text{PCC}} = i_{abc}^L + i_{abc}^{\text{CSC}}.
\]

Specifically for a CSC D-STATCOM, an LC filter is required to connect the current-source converter (CSC) with the electrical AC grid due to the PWM type of current. The mathematical model in state variables for the filter is given by:

\[
v_{abc}^{\text{PCC}} = L_C \frac{d}{dt} i_{abc}^L + v_{abc}^{\text{CSC}},
\]

\[
c_c \frac{d}{dt} v_{abc}^{\text{CSC}} = i_{abc}^{\text{CSC}} - i_{abc}^L,
\]

where $i_{abc}^{\text{CSC}}$ is the current injected by the CSC connected to the LC filter and it is defined by:

\[
i_{abc}^{\text{CSC}} = s_{abc} i_{dc}^s,
\]

and $s_{abc}$ is the CSC switching vector. Finally, the DC current can be written as:

\[
i_{dc} = \frac{d}{dt} i_{abc}^{\text{PCC}} = [s_{abc}]^T [v_{abc}^{\text{PCC}} - r_{dc} i_{dc}],
\]

where the resistance $r_{dc}$ is added to model the CSC losses, including DC inductor parasitic resistance and losses in the power valves. The current injected by the CSC has a PWM pattern. An average model can be used to reduce the analysis to the fundamental component, thus, $s_{abc}$ can be approximated as:

\[
s_{abc} \approx \mathbf{m} s_{abc},
\]

where $\mathbf{G}$ is the modulation technique gain for the fundamental component and $\mathbf{m}_{abc}$ is the vector of the CSC modulating signals. Finally, using the Park Transformation, the overall state model of the D-STATCOM is given by:

\[
\frac{d}{dt} i_{dc} = \frac{1}{L_c} (v_{abc}^{\text{PCC}} - v_{abc}^{\text{CSC}}) - W_i i_{dc}^c,
\]

\[
\frac{d}{dt} v_{abc}^c = \frac{1}{c_c} (i_{abc}^c - \mathbf{G} \mathbf{m} s_{dc}^i_{abc}) - W v_{abc}^d,
\]

\[
\frac{d}{dt} i_{abc}^c = \frac{1}{L_c} (\mathbf{G} \mathbf{m} s_{abc}^i - r_{dc} i_{dc}),
\]

where:

\[
\begin{align*}
\mathbf{v}_{\text{PCC}} & : \text{point of common coupling (PCC) voltage} \\
\mathbf{i}_{\text{PCC}} & : \text{point of common coupling (PCC) current} \\
\mathbf{i}_c & : \text{D-STATCOM current} \\
i_l & : \text{load current} \\
\mathbf{v}_c & : \text{D-STATCOM capacitor voltage}
\end{align*}
\]